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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant(s):	Kazunori KISHIMOTO
Serial No.:	10/083,447
Filed:	February 26, 2002
For:	METHOD OF TESTING A SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD AND APPARATUS FOR GENERATING TEST PATTERNS
Examiner:	John P. Trimmings
Group Art Unit:	2133
Attorney Docket No.:	NEKO 19.481 (100806-00091)

February 15, 2006

SUPPLEMENTAL BRIEF FOR APPELLANTS

Board of Patent Appeals and Interferences
Assistant Commissioner for Patents
Washington, D.C., 20231

Sir:

This Supplemental Brief for Appellants is submitted in response to the Notice of Non-Compliant Amendment dated February 9, 2006. This Supplemental Brief includes section X as required by 37 C.F.R. § 41.37.

A Notice of Appeal was filed on September 26, 2005. Appellant hereby petitions for a one-month extension of time, a petition pursuant to 37 C.F.R. § 1.136 (a) and authorization to charge the requisite fee being enclosed. Appellant hereby appeals to the Board of Patent Appeals and Interferences from the Examiner's Decision, in the Official Action dated April 29, 2005, finally rejecting claims 1-18, and from the Advisory Action dated August 9, 2005. All requisite fees, including those for this Brief set forth in 37 C.F.R. § 41.20(b)(2), may be charged to Deposit Account No. 50-1290.

I. Real party in interest

The real party in interest is NEC Electronics Corporation, a Japanese corporation with offices at 1753 Shimonumabe, Nakahara-Ku, Kawasaki, Kanagawa, Japan.

II. Related appeals and interferences

Upon information and belief, there are no other appeals or interferences, which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. Status of claims

Claims 1-18 are pending.

Claims 1-4, 6-11, and 13-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Appellant's allegedly admitted prior art (hereinafter referred to as the "AAAPA") in view of the IEEE publication "Test Generation for Crosstalk-Induced Delay in Integrated Circuits" by Chen, et al. (hereinafter referred to as the "Chen reference").

Claims 5, 12, and 16-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAAPA in view of the Chen reference and further in view of U.S. Patent No. 5,235,566 to Merrill (hereinafter referred to as the "Merrill Patent").

Claims 1-18 are appealed.

IV. Status of amendments

Appellant filed a response to the final Office Action on July 18, 2005, including an amendment of claim 14. The Advisory Action of August 9, 2005, indicates that the Examiner entered the amendment. Appellant did not otherwise cancel or amend any of the claims that are the subject of this appeal.

V. Summary of claimed subject matter

The independent claims in the present application provide that the propagation delay time on a measurement path is measured by comparing or evaluating the actual value of a register at the end of the measurement path with an expected value. (Specification; page 22, lines 19-23). In particular, claim 1 relates to a method for testing a semiconductor integrated circuit. When a signal for measuring a delay (for example, flip-flop 10m, shown in Figure 2a and discussed in the Specification; page 26, lines 2-4) is applied to a measurement path (shown in figures 2a and 3a), on which a delay test is conducted, a signal (for example, flip-flop 10n, shown in Figure 2a and discussed in the Specification; page 26, lines 6-8) having a transition being in phase or in opposite phase with the signal for measuring a delay applied to the measurement path is applied to a path that influences crosstalk (referred to in the figures as an aggressor path, shown in figures 2a and 3a), to the measurement path. In this manner, a propagation delay time of the

signal that propagates through the measurement path under the influence of crosstalk is measured. In the method according to claim 1, a propagation delay time of a signal is determined by comparing a value of a flip-flop (for example, flip-flop 10p, shown in Figure 2a and discussed in the Specification; page 32, lines 3-5) receiving the signal outputted from an output end of a measurement path with an expected value.

Independent claim 3 relates to a method for testing a semiconductor integrated circuit in an AC test using a scan path. (Specification; page 19, line 1 to page 21, line 23). The method includes receiving from a scan-in terminal of a scan path register (also referred to as flip-flops, see Specification; page 19, line 4) a pattern for supplying a signal for measuring a delay to a measurement path on which a delay test is conducted and a pattern for supplying a signal having a transition being in phase or in opposite phase with said signal for measuring a delay to a path that influences crosstalk to said measurement path. The method of claim 3 also includes supplying said signal for measuring a delay to said measurement path and supplying the signal to the path that influences crosstalk to said measurement path from said scan path register, and reading out a value of the scan path register that samples said signal at an end terminal of said measurement path, from a scan-out terminal to compare the value of said scan path register with an expected value, thereby measuring a delay time in said measurement path. (Specification; page 21, lines 11-13).

The present invention as recited in claim 4 relates to a method for testing a semiconductor integrated circuit having a scan path.

A method for testing a semiconductor integrated circuit having a scan path is recited in claim 5.

A method for generating patterns for testing a semiconductor integrated circuit having a scan path circuit by a computer is recited in claim 7.

A method for generating patterns for testing a semiconductor integrated circuit having a scan path circuit by a computer is recited in claim 8.

An apparatus for generating patterns for testing a semiconductor integrated circuit having a scan path circuit is recited in claim 9.

An apparatus for generating patterns for testing a semiconductor integrated circuit having a scan pass circuit is recited in claim 10.

A method for testing a semiconductor integrated circuit having a scan path circuit as a device under test with an LSI tester is recited in claim 11.

A method for testing a semiconductor integrated circuit having a scan path circuit as a device under test with an LSI tester as a testing device is recited in claim 12.

A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit is recited in claim 14.

A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit is recited in claim 15.

A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit is recited in claim 16.

All of the independent claims 1, 3-5, 7-12, and 14-16 include a feature of "comparing a value of a flip-flop receiving said signal outputted from an output end of said measurement path with an expected value" (Claims 1, 7, 8, 9, 10, 14), or a similar feature ("compare the value of said scan path register with an expected value, thereby measuring a delay time in said measurement path" (Claim 3), "comparing a value of a flip-flop that samples the signal of an end

terminal of said measurement path with an expected value, thereby measuring a delay time in said measurement path" (Claims 4 and 5), "comparing the value of the flip-flop that receives the outputted signal outputted from the output end of said measurement path at the data terminal thereof with an expected value" (Claims 11 and 12), and "comparing a value of a flip-flop receiving said signal propagated through said measurement path outputted from an output end of said measurement path with an expected value" (Claims 15 and 16)). This feature is discussed in the Specification at least at page 21, lines 11-13; page 29, line 4 to page 30, line 6; and page 32, lines 3-5.

VI. Grounds of rejection to be reviewed on appeal

1. Whether or not claims 1-4, 6-11, and 13-15 are unpatentable under 35 U.S.C. § 103(a) based on the AAAPA in view of the Chen reference.

2. Whether or not claims 5, 12, and 16-18 are unpatentable under 35 U.S.C. § 103 based on the AAAPA in view of the Chen reference and further in view of the Merrill Patent.

VII. Argument

1. Whether or not claims 1-4, 6-11, and 13-15 are unpatentable under 35 U.S.C. § 103(a) based on the AAAPA in view of the Chen reference.

a. There is no motivation to combine the AAAPA and the Chen reference

Claims 1-4, 6-11, and 13-15 are rejected based on the combination of the AAAPA and the Chen reference. However, there is no motivation to combine the references. The Office Action of April 29, 2005 maintains the rejections of the prior Office Action, which stated that "one with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the cost cutting teachings of Chen et al. to the prior art method and

program product based on the same." (Office Action of August 17, 2004; page 4, lines 9-18). However, this conclusory reasoning is insufficient to support a claim of obviousness. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either ***explicitly or implicitly in the references themselves or in the knowledge generally available*** to one of ordinary skill in the art. (MPEP 2143.01, emphasis added). "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

The Federal Circuit addressed the standard for obviousness and the requirement of motivation in Teleflex, Inc. et al. v. KSR Int'l Co., (119 Fed. Appx. 282; 2005 U.S. App. LEXIS 176). The patent at issue in *Teleflex*, related to an electronic pedal position control and a pedal assembly. In *Teleflex*, the district court granted a motion for summary judgment based on invalidity due to obviousness. The Federal Circuit vacated the decision and remanded to the lower court for further proceedings on the issue of obviousness. The Federal Circuit stated that, in regard to obviousness, "a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, ***but some motivation to combine the prior art teachings in the particular manner claimed.***" (*Teleflex*, citing *In re Kotzab*; emphasis added). The Federal Circuit found that that there was no motivation to combine the Asano patent, which disclosed all of the limitations except the electronic control, and the Rixon patent, which disclosed an electronic control and an adjustable pedal assembly. As the court further stated:

> [t]he district court correctly noted that the nature of the problem to be solved may, under appropriate circumstances, provide a suggestion or motivation to combine prior art references. However,

> the ***test requires that the nature of the problem to be solved be such that it would have led a person of ordinary skill in the art to combine the prior art teachings in the particular manner claimed***.

(*Teleflex*, citing as background *Rouffet*, 149 F.3d at 1357; emphasis added).

It is respectfully submitted that the present rejection is similar to the rejection discussed in *Teleflex* in that there is no motivation provided in the Chen reference to combine its teaching with the AAAPA. The Chen reference apparently discusses analyzing propagation delays due to cross-talk influences, and discusses advantages due to testing for cross-talk. However, there is no motivation in the Chen reference to suggest a combination with the testing regimen discussed in the AAAPA. As the *Teleflex* court held, there must be ***specific teaching*** to motivate a person of ordinary skill in the art must to combine the prior art teachings ***in the particular manner claimed***. Therefore, since there is no motivation to combine the references, the rejection is improper.

The Examiner uses an alleged advantage of the Chen reference, cost saving, as a motivation to combine the teaching of the Chen reference with the AAAPA, without showing that the AAAPA furthers this goal. A general statement of improvement, by for instance cost-savings or increased efficiency, does not translate into a motivation to combine references. The AAAPA relates to testing a semiconductor integrated circuit device by a scan path method. (Specification; page 1, line 15 to page 3, line 2). However, there is no indication that the AAAPA is a cost saving method. There is also no indication of the feasibility, much less the desirability, of combining the AAAPA with the Chen reference to arrive at the method of the present invention.

The Advisory Action of August 9, 2005 cites the Chen reference, page 191, column 2, as discussing testing as an alternative to redesigning a circuit, and therefore argues that cost saving

is the motivation for combining the Chen reference and the AAAPA. However, since all testing arguably results in cost savings, this reasoning would justify combining the Chen reference with any testing regimen, based on any technique. It is respectfully submitted that this reasoning masks the use of impermissible hindsight reasoning, as it clearly results in the viriation of the motivation requirement in the obvious rejection. The Chen reference does not provide any motivation for a skilled practitioner in the art to look to the AAAPA to combine the references.

b. Neither the Chen reference nor the AAAPA discloses or suggests comparing a value of a flip-flop receiving a signal outputted from an output end of a measurement path under the influence of crosstalk with an expected value.

Claims 1-4, 6-11, and 13-15 all include a feature of "comparing a value of a flip-flop receiving said signal outputted from an output end of said measurement path with an expected value" (Claims 1, 7, 8, 9, 10, 14), or a similar feature. ("compare the value of said scan path register with an expected value, thereby measuring a delay time in said measurement path" (Claim 3), "comparing a value of a flip-flop that samples the signal of an end terminal of said measurement path with an expected value, thereby measuring a delay time in said measurement path" (Claim 4), "comparing the value of the flip-flop that receives the outputted signal outputted from the output end of said measurement path at the data terminal thereof with an expected value" (Claim 11), and "comparing a value of a flip-flop receiving said signal propagated through said measurement path outputted from an output end of said measurement path with an expected value" (Claim 15)).

The Examiner admits that the Chen reference is relied on only "to make up the deficiency of the teaching of a second signal applied to influence crosstalk in a measurement circuit." (Advisory Action; page 2, lines 8-9). However, the AAAPA does not disclose, or even suggest,

measuring a propagation delay time of a signal that propagates through a measurement path under the influence of crosstalk by comparing a value of a flip-flop receiving a signal outputted from an output end of the measurement path with an expected value. The Examiner's combination of the references merely inserts "cross-talk", as supplied from the Chen reference, into the AAAPA. It is respectfully submitted that such a combination is improper and can only be the result of impermissible hindsight reasoning. Since none of the references disclose or suggest comparing a value of a flip-flop receiving a signal outputted from an output end of a measurement path under the influence of crosstalk with an expected value, the combination of the references does not render the claims unpatentable.

In view of the foregoing, it is respectfully submitted that claims 1-4, 6-11, and 13-15 are patentable over the AAAPA in view of the Chen reference for at least the above-stated reasons.

2. Whether or not claims 5, 12, and 16-18 are unpatentable under 35 U.S.C. § 103 based on the AAAPA in view of the Chen reference and further in view of the Merrill Patent.

a. There is no motivation to combine the AAAPA and the Chen reference

Claims 5, 12, and 16-18 are rejected based on the combination of the AAAPA in view of the Chen reference and further in view of the Merrill Patent. However, as discussed above there is no motivation to combine the AAAPA and the Chen reference. Therefore, the combination of the references is improper. The addition of the Merrill Patent does not cure the deficiency discussed above in regard to the lack of motivation to combine the AAAPA and the Chen reference. In particular, the Office Action of April 29, 2005 maintains the rejections of the prior Office Action, which stated that "[o]ne with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to combine the teachings of Merrill in order to measure the effects of the clock on the circuit of the prior art above." (Office Action of August

17, 2004; page 6, lines 2-5). However, this conclusory reasoning is also insufficient to support a claim of obviousness. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either ***explicitly or implicitly in the references themselves or in the knowledge generally available*** to one of ordinary skill in the art. (MPEP 2143.01, emphasis added). The Federal Circuit in *Teleflex* stated that, in regard to obviousness, "a person of ordinary skill in the art must not only have had some motivation to combine the prior art teachings, ***but some motivation to combine the prior art teachings in the particular manner claimed***." (*Teleflex*, citing *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000); emphasis added).

It is respectfully submitted that the present rejection is similar to the rejection discussed in *Teleflex* in that there is no motivation provided in the Merrill Patent to combine its teaching with the AAAPA and/or the Chen reference. The Merrill Patent apparently discusses a clock skew measurement technique. However, there is no motivation in the Merrill Patent to suggest combination with the testing regimen discussed in the AAAPA or the test generation for cross-talk discussed in the Chen reference. As the *Teleflex* court held, there must be ***specific teaching*** to motivate a person of ordinary skill in the art must to combine the prior art teachings ***in the particular manner claimed***. Therefore, since there is no motivation to combine the references, the rejection is improper.

b. None of the Chen reference, the AAAPA, nor the Merrill patent discloses or suggests comparing a value of a flip-flop that samples the signal of an end terminal of said measurement path with an expected value, thereby measuring a delay time in said measurement path.

Claims 5, 12, and 16-18 all include a feature of "comparing a value of a flip-flop that samples the signal of an end terminal of said measurement path with an expected value, thereby

measuring a delay time in said measurement path" (Claim 5), or a similar feature ("comparing the value of the flip-flop that receives the outputted signal outputted from the output end of said measurement path at the data terminal thereof with an expected value" (Claim 12), and "comparing a value of a flip-flop receiving said signal propagated through said measurement path outputted from an output end of said measurement path with an expected value" (Claim 16)).

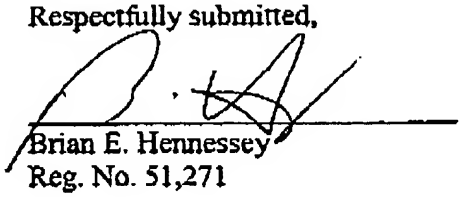
The Examiner admits that the Merrill Patent is relied on only to make up the deficiency of the teaching in the AAAPA and the Chen reference of "applying a signal to a path that influences crosstalk to the measurement path by affecting a clock." (Office Action of August 17, 2004; page 5, lines 17-19). Therefore, the rejection of this group of claims depends on the AAAPA and the Chen reference as disclosing this feature. However, as discussed above, the AAAPA does not disclose, or even suggest, measuring a propagation delay time of a signal that propagates through a measurement path under the influence of crosstalk by comparing a value of a flip-flop receiving a signal outputted from an output end of the measurement path with an expected value. The Examiner's combination of the references merely inserts "cross-talk", as supplied from the Chen reference, into the AAAPA. It is respectfully submitted that such a combination is improper and can only be the result of impermissible hindsight reasoning. Since none of the references disclose or suggest comparing a value of a flip-flop receiving a signal outputted from an output end of a measurement path under the influence of crosstalk with an expected value, the combination of the references does not render the claims unpatentable.

In view of the foregoing, it is respectfully submitted that claims 5, 12, and 16-18 are patentable over the AAAPA in view of the Chen reference and further in view of the Merrill Patent for at least the above-stated reasons.

CONCLUSION

Claims 1-4, 6-11, and 13-15 are patentable over the AAAPA in view of the Chen reference, and claims 5, 12, and 16-18 are patentable over the AAAPA in view of the Chen reference and further in view of the Merrill Patent. Accordingly, it is respectfully submitted that the Examiner erred in rejecting claims 1-18 and a reversal of such rejections by this Honorable Board is solicited.

Respectfully submitted,



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VIII. Claims Appendix

1. A method for testing a semiconductor integrated circuit, wherein, when a signal for measuring a delay is applied to a measurement path on which a delay test is conducted, a signal having a transition being in phase or in opposite phase with said signal for measuring a delay applied to said measurement path is applied to a path that influences crosstalk to said measurement path, thereby measuring a propagation delay time of said signal that propagates through said measurement path under the influence of crosstalk, said propagation delay time of said signal being determined by comparing a value of a flip-flop receiving said signal outputted from an output end of said measurement path with an expected value.

2. The method according to claim 1, further comprising the steps of:

supplying said signal for measuring a delay to said measurement path after a signal level of said path that influences crosstalk to said measurement path is set to a fixed value, thereby, measuring the propagation delay time of said signal for measuring a delay that propagates through said measurement path; and

performing a quantitative evaluation on the influence of crosstalk, on the basis of a difference between the propagation delay time measured after the signal level of said path that influences crosstalk to said measurement path is set to the fixed value and the propagation delay time of said signal for measuring a delay, measured with the signal applied to said path that influences crosstalk to said measurement path.

3. A method for testing a semiconductor integrated circuit in an AC test using a scan path, the method comprising the steps of:

receiving from a scan-in terminal of a scan path register a pattern for supplying a signal for measuring a delay to a measurement path on which a delay test is conducted and a pattern for supplying a signal having a transition being in phase or in opposite phase with said signal for measuring a delay to a path that influences crosstalk to said measurement path;

supplying said signal for measuring a delay to said measurement path and supplying the signal to the path that influences crosstalk to said measurement path from said scan path register; and

reading out a value of the scan path register that samples said signal at an end terminal of said measurement path, from a scan-out terminal to compare the value of said scan path register with an expected value, thereby measuring a delay time in said measurement path.

4. A method for testing a semiconductor integrated circuit having a scan path, the method comprising the steps of:

supplying a signal for measuring a delay to a measurement path of a combinational circuit from a flip-flop associated with said measurement path, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting the scan path, and also supplying to an aggressor path that influences crosstalk to said measurement path a signal having a transition being in phase or in opposite phase with said signal supplied to said measurement path from a flip-flop associated with the aggressor path; and

comparing a value of a flip-flop that samples the signal of an end terminal of said measurement path with an expected value, thereby measuring a delay time in said measurement path.

5. A method for testing a semiconductor integrated circuit having a scan path, the method comprising the steps of:

supplying a signal for measuring a delay to a measurement path in a combinational circuit from a flip-flop associated with said measurement path, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting the scan path, and also supplying to a path that influences crosstalk to a clock signal path a signal having a transition being in phase or in opposite phase with said clock signal, a clock to one or

plural flip-flop associated with said measurement path being supplied through said clock signal path; and

comparing a value of the flip-flop that samples the signal at an end terminal of said measurement path with an expected value, thereby measuring a delay time in said measurement path.

6. The method according to claim 4, further comprising the steps of:

supplying a signal for setting said aggressor path that influences crosstalk to said measurement path to a fixed value from the flip-flop associated with said aggressor path so as to measure a delay time in said measurement path; and

evaluating an effect of crosstalk on the basis of a difference between the delay time in said measurement path measured after the signal for setting said aggressor path to the fixed value is applied and the delay time in said measurement path measured with the signal applied to said aggressor path that influences crosstalk to said measurement path.

7. A method for generating patterns for testing a semiconductor integrated circuit having a scan path circuit by a computer, the method comprising the steps of:

generating information on an aggressor path that influences crosstalk to a measurement path of a combinational circuit for measuring a delay, on the basis of layout information on said semiconductor integrated circuit, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path; and

generating a pattern for causing a flip-flop associated with said measurement path to output a signal supplied to said measurement path for measuring a delay, and generating a pattern for causing a flip-flop associated with said aggressor path to output a signal supplied to said aggressor path for checking on influence of crosstalk to said measurement path, said delay being determined by comparing a value of a flip-flop receiving said signal supplied to said

measurement path outputted from an output end of said measurement path with an expected value.

8. A method for generating patterns for testing a semiconductor integrated circuit having a scan path circuit by a computer, the method comprising the steps of:

(a) extracting one or plural adjacent paths on the basis of layout information on said semiconductor integrated circuit to extract information on a path that influences crosstalk;

(b) generating measurement path information on a measurement path in a combinational circuit for measuring a delay, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path, said measurement path information including a combination of nodes constituting said measurement path and transition information of a signal at respective nodes, and generating aggressor path information comprising node information on an aggressor path that influences crosstalk to said measurement path, by referring to said extracted information on crosstalk; and

(c) generating a pattern for outputting a signal that should be set for allowing a signal for measuring a delay supplied to said measurement path to propagate through said measurement path, said pattern being outputted from an associated flip-flop of a register on an input side of said measurement path, and generating a pattern for outputting a signal that should be set so as to be supplied to said aggressor path for influencing crosstalk to said measurement path for propagation through said aggressor path from an associated flip-flop of a register on an input side of said aggressor path, on the basis of circuit information on said semiconductor integrated circuit, said measurement path information, and said aggressor path information, said delay being determined by comparing a value of a flip-flop receiving said signal propagating through said measurement path outputted from an output end of said measurement path with an expected value.

9. An apparatus for generating patterns for testing a semiconductor integrated circuit having a scan path circuit, the apparatus comprising:

means for generating information on an aggressor path that influences crosstalk to a measurement path of a combinational circuit for measuring a delay, on the basis of layout information on said semiconductor integrated circuit, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path; and

means for generating a pattern for causing a flip-flop associated with said measurement path to output a signal supplied to said measurement path for measuring a delay, and generating a pattern for causing a flip-flop associated with said aggressor path to output a signal supplied to said aggressor path for checking on influence of crosstalk to said measurement path, said delay being determined by comparing a value of a flip-flop receiving said signal supplied to said measurement path outputted from an output end of said measurement path with an expected value.

10. An apparatus for generating patterns for testing a semiconductor integrated circuit having a scan pass circuit, the apparatus comprising:

means for extracting adjacent wiring paths on the basis of layout information on said semiconductor integrated circuit to extract information on a path that influences crosstalk;

means for generating measurement path information on a measurement path of a combinational circuit for measuring a delay, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path, said measurement path information comprising a combination of nodes constituting said measurement path and transition information of a signal at the nodes, and generating aggressor path information comprising node information on the path that influences crosstalk to said measurement path, by referring to said extracted information on crosstalk; and

means for generating a pattern for outputting a signal that should be set for allowing a signal for measuring the delay to propagate through said measurement path, said pattern being outputted from an associated flip-flop of a register on an input side of said measurement path, and generating a pattern for outputting a signal that should be set so as to be supplied to said aggressor path for influencing crosstalk to said measurement path for propagation through said aggressor path from an associated flip-flop of a register on an input side of said aggressor path, on the basis of circuit information on said semiconductor integrated circuit, said measurement path information, and said aggressor path information, the delay being determined by comparing a value of a flip-flop receiving said signal propagated through said measurement path outputted from an output end of said measurement path with an expected value.

11. A method for testing a semiconductor integrated circuit having a scan path circuit as a device under test with an LSI tester, the method comprising:

(a) a first step for setting said semiconductor integrated circuit to a scan mode to serially supply from a scan-in terminal on said semiconductor integrated circuit initialization patterns,

said initialization patterns including:

a pattern for initializing a flip-flop with an output terminal thereof connected to an input terminal of a measurement path in a combinational circuit for measuring a delay and an aggressor path that influences crosstalk to said measurement path, respectively, the combinational circuit having an input terminal thereof connected to an output terminal of a register comprised of one or plural flip-flops constituting a scan path and an output terminal thereof connected to an input terminal of a register comprised of one or plural flip-flops constituting said scan parh;

a pattern for setting one or plural flip-flops that should be set so as to influence statuses of the input terminals of said measurement path and said aggressor path to undergo transitions from the initial states to predetermined states, the one or plural flip-flops being connected through a combinational circuit to data input terminals of said flip-flops; and

a pattern for setting one or plural flip-flops that should be set so as to cause signals to propagate through said measurement path and said aggressor path to predetermined states;

(b) a second step for setting said semiconductor integrated circuit from the scan mode to a normal mode to cause the flip-flop that outputs the signal to the input terminal of said measurement path to latch a signal applied to a data input end thereof on a first clock, thereby causing the output signal thereof to be changed from the initial state and also to cause the flip-flop that outputs the signal to the input end of said aggressor path to latch a signal applied to a data input terminal thereof on the first clock, thereby causing the output signal thereof to be changed from the initial state, and then causing the flip-flop that receives at a data input terminal thereof the signal at an output end of said measurement path to receive the outputted signal at the data input terminal thereof on a second clock;

(c) a third step for setting said semiconductor integrated circuit to the scan mode again to read out values of the flip-flops that constitutes the scan path from a scan-out terminal arranged on said semiconductor integrated circuit, and then comparing the value of the flip-flop that receives the outputted signal outputted from the output end of said measurement path at the data terminal thereof with an expected value; and

(d) decreasing a clock period by a predetermined period of time if a result of said comparison is a pass, and increasing the clock period by a predetermined period of time if the result of said comparison is a fail, executing the first, second, and third steps, and then determining the clock period at a transition time when the result of said comparison has changed from the pass to the fail, or from the fail to the pass, to be the delay time in said measurement path under the influence of crosstalk.

12. A method for testing a semiconductor integrated circuit having a scan path circuit as a device under test with an LSI tester as a testing device, the method comprising:

(a) a first step for setting said semiconductor integrated circuit to a scan mode to serially supply from a scan-in terminal on said semiconductor integrated circuit initialization patterns,

said initialization patterns including:

a pattern for initializing a flip-flop with an output terminal thereof connected to an input terminal of a measurement path of a combinational circuit for measuring a delay, said combinational circuit having an input terminal thereof connected to an output terminal of a register comprising one or plural flip-flops constituting a scan path and an output terminal thereof connected to an input terminal of a register comprising one or plural flip-flops constituting said scan path;

a pattern for initializing a flip-flop connected to a path that influences crosstalk to a clock signal path for supplying a clock to a flip-flop connected to said measurement path, said path that influences crosstalk being hereinafter referred to as an aggressor path;

a pattern for setting one or plural flip-flops that should be set so as to cause a status of the input terminal of said measurement path to be changed from the initial state, to predetermined states, the one or plural flip-flops being connected to respective data terminals of said flip-flops through a combinational circuit;

a pattern for setting one or plural flip-flops that should be set so as to cause an input terminal of said aggressor path to be changed from the initial state to a state in phase or in opposite phase with the clock, to predetermined states; and

patterns for setting one or plural flip-flops that should be set so as to cause signals to propagate through said measurement path and said aggressor path to predetermined states;

(b) a second step for setting said semiconductor integrated circuit from the scan mode to a normal mode to cause the flip-flop that outputs the signal to the input end of said measurement path to latch a signal applied to a data input terminal thereof on a first clock, thereby causing the output signal to be changed from the initial state and also to cause the flip-flop that outputs the signal to the input terminal of said aggressor path to latch a signal applied to a data input terminal thereof on the first clock, thereby causing the output signal to be changed from the initial state, and then causing the flip-flop that receives from a data input terminal thereof the

signal at an output end of said measurement path to receive the output signal at the data input terminal thereof on a second clock;

(c) a third step for setting said semiconductor integrated circuit to the scan mode again to read out values of the flip-flops that constitutes the scan path from a scan-out terminal on said semiconductor integrated circuit, and then comparing the value of the flip-flop that receives the outputted signal outputted from the output terminal of said measurement path at the data terminal thereof with an expected value; and

(d) a fourth step for decreasing a clock period by a predetermined period of time if a result of said comparison is a pass, and increasing the clock period by a predetermined period of time if the result of said comparison is a fail, executing the first, second, and third steps, and then determining the clock period at a transition time when the result of said comparison has changed from the pass to the fail, or from the fail to the pass, to be the delay time in said measurement path with an effect of crosstalk.

13. The method according to claim 11, further comprising the steps of:

supplying a signal for setting said path that influences crosstalk to said measurement path to a fixed value from the flip-flop associated with the path so as to measure a delay time in said measurement path; and

evaluating the influence of crosstalk on the basis of a difference between the delay time in said measurement path measured after the signal for setting said path to the fixed value is supplied and the delay time in said measurement path measured with the signal supplied to said path that influences crosstalk to said measurement path.

14. A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit, the program product comprising the processes of:

(a) generating information on an aggressor path that influences crosstalk to a measurement path of a combinational circuit for measuring a delay, on the basis of layout information on said semiconductor integrated circuit, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path; and

(b) generating a pattern for causing a flip-flop associated with said measurement path to output a signal supplied to said measurement path for measuring a delay, and generating a pattern for causing a flip-flop associated with said aggressor path to output a signal supplied to said aggressor path for checking on influence of crosstalk to said measurement path, said delay being determined by comparing a value of a flip-flop receiving said signal supplied to said measurement path outputted from an output end of said measurement path with an expected value.

15. A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit, the program product comprising the processes of:

(a) extracting adjacent one or plural paths on the basis of layout information on said semiconductor integrated circuit to extract information on a path that influences crosstalk;

(b) generating measurement path information on a measurement path of a combinational circuit for measuring a delay, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path, said measurement path information comprising a combination of nodes constituting said measurement path and transition information of a signal at the nodes, and generating path information comprising node information on an aggressor path that influences crosstalk to said measurement path, by referring to said extracted information on crosstalk; and

(c) generating a pattern for outputting a signal that should be set for allowing a signal for measuring a delay to propagate through said measurement path, said pattern being outputted

from an associated flip-flop of a register on an input side of said measurement path, and generating a pattern for outputting a signal that should be set so as to be supplied to said aggressor path for influencing crosstalk to said measurement path and for propagation through said aggressor path from an associated flip-flop of a register on an input side of said aggressor path, on the basis of circuit information on said semiconductor integrated circuit, said measurement path information, and said aggressor path information, the delay being determined by comparing a value of a flip-flop receiving said signal propagated through said measurement path outputted from an output end of said measurement path with an expected value.

16. A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit, the program product comprising the processes of:

(a) extracting adjacent one or plural paths on the basis of layout information on said semiconductor integrated circuit to extract information on a path that influences crosstalk;

(b) generating measurement path information on a measurement path of a combinational circuit for measuring a delay, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path, said measurement path information comprising a combination of nodes constituting said measurement path and transition information of a signal at the nodes, and generating path information comprising node information on an aggressor path that influences crosstalk to a clock signal path for supplying a clock to a flip-flop associated with said measurement path, if said path exists, said path that influences crosstalk, by referring to said extracted information on crosstalk; and

(c) automatically generating a pattern for outputting the signal that should be set for allowing a signal for measuring the delay to propagate through said measurement path from an associated flip-flop of a register on an input side of said measurement path, and generating a pattern for outputting a signal that should be set so as to be supplied to said aggressor path for

influencing crosstalk to said measurement path for propagation through said aggressor path from an associated flip-flop of a register on an input side of said aggressor path, on the basis of circuit information on said semiconductor integrated circuit, said measurement path information and said clock signal path information, and said aggressor path information, the delay being determined by comparing a value of a flip-flop receiving said signal propagated through said measurement path outputted from an output end of said measurement path with an expected value.

17. The method according to claim 5, further comprising the steps of:

supplying a signal for setting said path that influences crosstalk to said measurement path to a fixed value from the flip-flop associated with said path so as to measure the delay in said measurement path; and

evaluating an effect of crosstalk on the basis of a difference between the delay in said measurement path measured after the signal for setting said path to the fixed value is applied and the delay in said measurement path measured with the signal applied to said path that influences crosstalk to said measurement path.

18. The method according to claim 12, further comprising the steps of:

supplying a signal for setting said path that influences crosstalk to said measurement path to a fixed value from the flip-flop associated with the path so as to measure the delay in said measurement path; and

evaluating the influence of crosstalk on the basis of a difference between the delay in said measurement path measured after the signal for setting said path to the fixed value is supplied and the delay in said measurement path measured with the signal supplied to said path that influences crosstalk to said measurement path.

IX. Evidence Appendix

No evidence was submitted to or entered by the Examiner during prosecution of this application.

X. Related Proceedings Appendix

No appeals or interferences, which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, are identified in section II of this brief, and therefore there are no decisions rendered by a court or the Board in any proceeding included in this section.